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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/517,258	12/07/2004	Katsuhiro Nakai	2004_1946A	1207

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WENDEROTH, LIND & PONACK, L.L.P.
2033 K STREET N. W.
SUITE 800
WASHINGTON, DC 20006-1021

EXAMINER	
OKORONKWO, CHINWENDU C	
ART UNIT	PAPER NUMBER
2136	

MAIL DATE	DELIVERY MODE
07/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/517,258	NAKAI ET AL.	
	Examiner	Art Unit	
	CHINWENDU C. OKORONKWO	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) *19-50* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20070823 and 20050210*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(a)-(e) or under 35 U.S.C. 120, 121, or 365(c) is acknowledged. Priority is claimed from Foreign Application No. 2002-174883 (Japan) and from PCT Application PCT/JP03/07541.

Information Disclosure Statement

2. For the record, the Examiner acknowledges the IDS submitted on 02/10/2005 and 08/23/2007. It has been received and considered.

Oath/Declaration

3. For the record, the Examiner acknowledges that the Oath/Declaration submitted on 12/07/2004 has been received and considered.

Drawings

4. For the record, the Examiner acknowledges that the Drawings submitted on 12/07/2004 have been received and considered.

5. Pursuant to USC 131, claims 1-18 are presented for examination.

6. Claims 1-18 are pending.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-18 are rejected under 35 U.S.C. 102() as being disclosed by Richards et al. (U.S. Patent No. 6,230,267).

Regarding claims 1, 7-8, 14, 16 and 18, Richards et al., discloses a semiconductor integrated circuit device having a second storage means in a semiconductor integrated circuit:

- in which a program that makes an arithmetic processing unit in the semiconductor integrated circuit perform an operation of processing contents is rewritably stored, and performing rewriting of the program stored in the second storage means using a first storage means in which a rewrite program for rewriting is stored, which rewrite program makes the arithmetic processing unit perform an operation of processing the contents (Figure 1A and 5:65-67 and 6:1-3 – "application provider" equated to the first storage means "initiates an application loading process onto IC card 103 … [t]he application provider 101 … desires to send and load an application to the IC card");

- wherein said second storage means has an externally readable area that can be read from the outside of the semiconductor integrated circuit, and an externally unreadable area that cannot be read from the outside and after arbitrary data is stored in the externally readable area of the second storage means, the data is read to the outside of the semiconductor integrated circuit to check whether the arbitrary data is the data as inputted, and thereafter, the rewrite program read from the first storage means is stored in the externally unreadable area of the second storage means (Figure 1A elements 15-19 and 5:51-61 – "data can be processed by the IC card 3. Only the IC card 3 has a copy of its private key so only the intended IC card can access the encrypted data. This ensures that third parties cannot access the encrypted data and correspondingly that only the intended IC card will be able to read and process the data").

Regarding claims 2 and 9, Richards et al., discloses semiconductor integrated circuit device having a second storage means in a semiconductor integrated circuit:

- in which a program that makes an arithmetic processing unit in the semiconductor integrated circuit perform an operation of processing contents is rewritably stored, and performing rewriting of the program stored in the second storage means using a first storage means in which a rewrite program for rewriting is stored, which rewrite program makes the

arithmetic processing unit perform an operation of processing the contents wherein said second storage means has an externally readable area that can be read from the outside of the semiconductor integrated circuit, and an externally unreadable area that cannot be read from the outside (Figure 2 and 6:34-42 – "Application Unit (AU) 203 … [which] contains the application code and data which are to stored on the IC card, some or all of which is encrypted to protect a secret portion or portions of the code and/or data.") and after arbitrary data is stored in the externally readable area of the second storage means, the data is read to the outside of the semiconductor integrated circuit to check whether the arbitrary data is the data as inputted, and thereafter, the rewrite program read from the first storage means is stored in the externally unreadable area of the second storage means (Figure 1A elements 15-19 and 5:51-61 – "data can be processed by the IC card 3. Only the IC card 3 has a copy of its private key so only the intended IC card can access the encrypted data. This ensures that third parties cannot access the encrypted data and correspondingly that only the intended IC card will be able to read and process the data").

Regarding claims 3-4, 10 and 17, Richards et al., discloses a semiconductor integrated circuit device wherein said control circuit performs control so as to read only the rewrite program located in specific addresses of the second

storage means (8:65-67 – "public key of an IC card is freely available to anyone and can be obtained from the card directly ... [whereas] only the intended IC card can use its secret key of the public/secret key pair … identify the encrypted portions of the application being loaded and use the keys to decrypt and recover the entire application and associate data. Because no other entity has the secret key of the IC card, the security and integrity of the [application] and data being transmitted is ensured.").

Regarding claims 5 and 11, Richards et al., discloses semiconductor integrated circuit device having a second storage means in a semiconductor integrated circuit:

- in which a program that makes an arithmetic processing unit in the semiconductor integrated circuit perform an operation of processing contents is rewritably stored, and performing rewriting of the program stored in the second storage means using a first storage means in which a rewrite program for rewriting is stored, which rewrite program makes the arithmetic processing unit perform an operation of processing the contents (Figure 1A and 5:65-67 and 6:1-3 – "application provider" equated to the first storage means "initiates an application loading process onto IC card 103 … [t]he application provider 101 … desires to send and load an application to the IC card");

- wherein said rewrite program includes a program for executing a portion of the rewrite program after the rewriting and the portion of the rewrite program stored in the second storage means is executed (8:65-67 – "public key of an IC card is freely available to anyone and can be obtained from the card directly ... [whereas] only the intended IC card can use its secret key of the public/secret key pair …[to] identify the encrypted portions of the application being loaded and use the keys to decrypt and recover the entire application and associate data. Because no other entity has the secret key of the IC card, the security and integrity of the [application] and data being transmitted is ensured." And 9:28-31 – "feild allows the microprocessor on the IC card to know how large an area has been encrypted and when coupled with the start of the area, allows the IC card microprocessor to decrypt the correct portion")

Regarding claims 6 and 12-13, Richards et al., discloses a semiconductor integrated circuit device wherein the portion of the rewrite program to be executed is one for successively executing discontinuous program areas (Figure 2 and 6:34-42 – "Application Unit (AU) 203 … [which] contains the application code and data which are to stored on the IC card, some or all of which is encrypted to protect a secret portion or portions of the code and/or data.")

Regarding claim 15, Richards et al., discloses semiconductor integrated circuit device as defined in claim 1 further including, in the semiconductor integrated circuit, a decryption means for decrypting the encrypted rewrite program; wherein, when the rewrite program stored in the first storage means has previously been encrypted, the decryption means decrypts the encrypted program, and stores the decrypted rewrite program in the second storage means (11:42-46 – "decrypts the identified portion with the identified decryption technique. This allows the IC card to have the decrypted portion of the AU which it will stored in its EEPROM once all the encrypted portions have been decrypted.").

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHINWENDU C. OKORONKWO whose telephone number is (571)272-2662. The examiner can normally be reached on MWF 2:30 - 6:00, TR 9:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami can be reached on (571) 272 4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. C. O./
Examiner, Art Unit 2136

/Nasser G Moazzami/
Supervisory Patent Examiner, Art Unit 2136